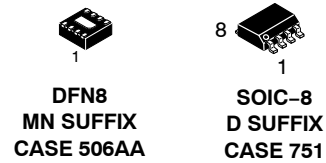


2.5 V / 3.3 V / 5.0 V 1:4 Clock Fanout Buffer

NB3L553



Description

The NB3L553 is a low skew 1-to 4 clock fanout buffer, designed for clock distribution in mind. The NB3L553 specifically guarantees low output-to-output skew. Optimal design, layout and processing minimize skew within a device and from device to device.

Features

- Input/Output Clock Frequency up to 200 MHz
- Low Skew Outputs (35 ps), Typical
- RMS Phase Jitter (12 kHz – 20 MHz): 29 fs (Typical)
- Output goes to Three-State Mode via OE
- Operating Range: $V_{DD} = 2.375\text{ V to }5.25\text{ V}$
- 5 V Tolerant Input Clock I_{CLK}
- Ideal for Networking Clocks
- Packaged in 8-pin SOIC
- Industrial Temperature Range
- These are Pb-Free Devices

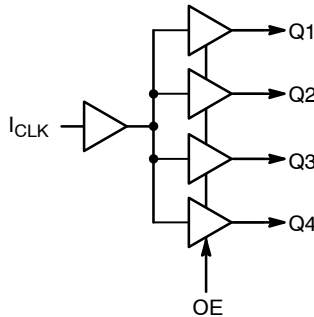
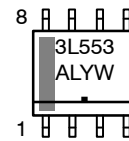
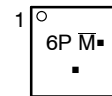


Figure 1. Block Diagram

MARKING DIAGRAM



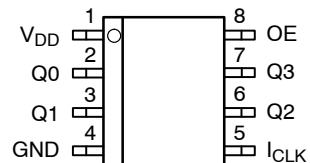
- 3L553 = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package



- 6P = Specific Device Code
 - M = Date Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

PINOUT DIAGRAM



ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|------------------|------------------|
| NB3L553DG | SOIC-8 (Pb-Free) | 98 Units/Rail |
| NB3L553DR2G | SOIC-8 (Pb-Free) | 2500/Tape & Reel |
| NB3L553MNR4G | DFN-8 (Pb-Free) | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NB3L553

Table 1. OE, OUTPUT ENABLE FUNCTION

| OE | Function |
|----|----------|
| 0 | Disable |
| 1 | Enable |

Table 2. PIN DESCRIPTION

| Pin # | Name | Type | Description |
|-------|------------------|-------------------------|---|
| 1 | V _{DD} | Power | Positive supply voltage (2.375 V to 5.25 V) |
| 2 | Q0 | (LV)CMOS/(LV)TTL Output | Clock Output 0 |
| 3 | Q1 | (LV)CMOS/(LV)TTL Output | Clock Output 1 |
| 4 | GND | Power | Negative supply voltage; Connect to ground, 0 V |
| 5 | I _{CLK} | (LV)CMOS Input | Clock Input. 5.0 V tolerant |
| 6 | Q2 | (LV)CMOS/(LV)TTL Output | Clock Output 2 |
| 7 | Q3 | (LV)CMOS/(LV)TTL Output | Clock Output 3 |
| 8 | OE | (LV)TTL Input | V _{DD} for normal operation. Pin has no internal pullup or pull down resistor for open condition default. Use from 1 to 10 kOhms external resistor to force an open condition default state. |
| - | EP | Thermal Exposed Pad | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

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Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|---|------------------------|--|---|--------------|
| V _{DD} | Positive Power Supply | GND = 0 V | – | 6.0 | V |
| V _I | Input Voltage | OE I _{CLK} | GND = 0 V and V _{DD} = 2.375 V to 5.25 V | GND – 0.5 ≤ V _I ≤ V _{DD} + 0.5 GND – 0.5 ≤ V _I ≤ 5.75 | V |
| T _A | Operating Temperature Range, Industrial | – | – | ≥ –40 to ≤ +85 | °C |
| T _{stg} | Storage Temperature Range | – | – | –65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction–to–Ambient) | 0 lfpm 500 lfpm | SOIC–8 | 190 130 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction–to–Case) | (Note 1) | SOIC–8 | 41 to 44 | °C/W |
| θ _{JA} | Thermal Resistance (Junction–to–Ambient) | 0 lfpm 500 lfpm | DFN8 DFN8 | 129 84 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction–to–Case) | (Note 1) | DFN8 | 35 to 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. ATTRIBUTES

| Characteristic | Value |
|---|---|
| ESD Protection | Human Body Model Machine Model Charged Device Model |
| | > 2 kV > 150 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2) | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 |
| | UL–94 code V–0 @ 0.125 in |
| Transistor Count | 531 Devices |
| Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test | |

2. For additional Moisture Sensitivity information, refer to Application Note [AND8003/D](#).

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Table 5. DC CHARACTERISTICS ($V_{DD} = 2.375\text{ V to }2.625\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|--|-------------------------|----------|-------------------------|----------|
| I_{DD} | Power Supply Current @ 135 MHz, No Load | - | 25 | 30 | mA |
| V_{OH} | Output HIGH Voltage – $I_{OH} = -16\text{ mA}$ | 1.7 | - | - | V |
| V_{OL} | Output LOW Voltage – $I_{OL} = 16\text{ mA}$ | - | - | 0.4 | V |
| V_{IH}, I_{CLK} | Input HIGH Voltage, I_{CLK} | $(V_{DD} \div 2) + 0.5$ | - | 5.0 | V |
| V_{IL}, I_{CLK} | Input LOW Voltage, I_{CLK} | - | - | $(V_{DD} \div 2) - 0.5$ | V |
| V_{IH}, OE | Input HIGH Voltage, OE | 1.8 | - | V_{DD} | V |
| V_{IL}, OE | Input LOW Voltage, OE | - | - | 0.7 | V |
| ZO | Nominal Output Impedance | - | 20 | - | Ω |
| CIN | Input Capacitance, I_{CLK} , OE | - | 5.0 | - | pF |
| IOS | Short Circuit Current | - | ± 28 | - | mA |

DC CHARACTERISTICS ($V_{DD} = 3.15\text{ V to }3.45\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|---|-------------------------|----------|-------------------------|----------|
| I_{DD} | Power Supply Current @ 135 MHz, No Load | - | 35 | 40 | mA |
| V_{OH} | Output HIGH Voltage – $I_{OH} = -25\text{ mA}$ | 2.4 | - | - | V |
| V_{OL} | Output LOW Voltage – $I_{OL} = 25\text{ mA}$ | - | - | 0.4 | V |
| V_{OH} | Output HIGH Voltage – $I_{OH} = -12\text{ mA}$ (CMOS level) | $V_{DD} - 0.4$ | - | - | V |
| V_{IH}, I_{CLK} | Input HIGH Voltage, I_{CLK} | $(V_{DD} \div 2) + 0.7$ | - | 5.0 | V |
| V_{IL}, I_{CLK} | Input LOW Voltage, I_{CLK} | - | - | $(V_{DD} \div 2) - 0.7$ | V |
| V_{IH}, OE | Input HIGH Voltage, OE | 2.0 | - | V_{DD} | V |
| V_{IL}, OE | Input LOW Voltage, OE | 0 | - | 0.8 | V |
| ZO | Nominal Output Impedance | - | 20 | - | Ω |
| CIN | Input Capacitance, OE | - | 5.0 | - | pF |
| IOS | Short Circuit Current | - | ± 50 | - | mA |

DC CHARACTERISTICS ($V_{DD} = 4.75\text{ V to }5.25\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|---|-----------------------|----------|-----------------------|----------|
| I_{DD} | Power Supply Current @ 135 MHz, – No Load | - | 45 | 85 | mA |
| V_{OH} | Output HIGH Voltage – $I_{OH} = -35\text{ mA}$ | 2.4 | - | - | V |
| V_{OL} | Output LOW Voltage – $I_{OL} = 35\text{ mA}$ | - | - | 0.4 | V |
| V_{OH} | Output HIGH Voltage – $I_{OH} = -12\text{ mA}$ (CMOS level) | $V_{DD} - 0.4$ | - | - | V |
| V_{IH}, I_{CLK} | Input HIGH Voltage, I_{CLK} | $(V_{DD} \div 2) + 1$ | - | 5.0 | V |
| V_{IL}, I_{CLK} | Input LOW Voltage, I_{CLK} | - | - | $(V_{DD} \div 2) - 1$ | V |
| V_{IH}, OE | Input HIGH Voltage, OE | 2.0 | - | V_{DD} | V |
| V_{IL}, OE | Input LOW Voltage, OE | - | - | 0.8 | V |
| ZO | Nominal Output Impedance | - | 20 | - | Ω |
| CIN | Input Capacitance, OE | - | 5.0 | - | pF |
| IOS | Short Circuit Current | - | ± 80 | - | mA |

NB3L553

Table 6. AC CHARACTERISTICS; $V_{DD} = 2.5\text{ V} \pm 5\%$ ($V_{DD} = 2.375\text{ V}$ to 2.625 V , $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|------------|--|-----|-----|-----|------|
| f_{in} | Input Frequency | – | – | 200 | MHz |
| t_r/t_f | Output rise and fall times; 0.8 V to 2.0 V | – | 1.0 | 1.5 | ns |
| t_{pd} | Propagation Delay, CLK to Q_n (Note 4) | 2.2 | 3.0 | 5.0 | ns |
| t_{skew} | Output-to-output skew; (Note 5) | – | 35 | 50 | ps |
| t_{skew} | Device-to-device skew, (Note 5) | – | – | 500 | ps |

AC CHARACTERISTICS; $V_{DD} = 3.3\text{ V} \pm 5\%$ ($V_{DD} = 3.15\text{ V}$ to 3.45 V , $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Conditions | Min | Typ | Max | Unit |
|--------------------|---|--------------------------------|-----|-----|-----|------|
| f_{in} | Input Frequency | | – | – | 200 | MHz |
| $t_{jitter}(\phi)$ | RMS Phase Jitter (Integrated 12 kHz – 20 MHz) (See Figures 2 and 3) | $f_{carrier} = 100\text{ MHz}$ | – | 18 | – | fs |
| t_r/t_f | Output rise and fall times; 0.8 V to 2.0 V | | – | 0.6 | 1.0 | ns |
| t_{pd} | Propagation Delay, CLK to Q_n (Note 4) | | 2.0 | 2.4 | 4.0 | ns |
| t_{skew} | Output-to-output skew; (Note 5) | | – | 35 | 50 | ps |
| t_{skew} | Device-to-device skew, (Note 5) | | – | – | 500 | ps |

AC CHARACTERISTICS; $V_{DD} = 5.0\text{ V} \pm 5\%$ ($V_{DD} = 4.75\text{ V}$ to 5.25 V , $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 3)

| Symbol | Characteristic | Min | Min | Typ | Max | Unit |
|--------------------|---|-----|--------------------------------|-----|-----|------|
| f_{in} | Input Frequency | | – | – | 200 | MHz |
| $t_{jitter}(\phi)$ | RMS Phase Jitter (Integrated 12 kHz – 20 MHz) (See Figures 2 and 3) | | $f_{carrier} = 100\text{ MHz}$ | 29 | – | fs |
| t_r/t_f | Output rise and fall times; 0.8 V to 2.0 V | | – | 0.3 | 0.7 | ns |
| t_{pd} | Propagation Delay, CLK to Q_n (Note 4) | | 1.7 | 2.5 | 4.0 | ns |
| t_{skew} | Output-to-output skew; (Note 5) | | – | 35 | 50 | ps |
| t_{skew} | Device-to-device skew, (Note 5) | | – | – | 500 | ps |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Outputs loaded with external $R_L = 33\ \Omega$ series resistor and $C_L = 15\text{ pF}$ to GND. Duty cycle out = duty in. A $0.01\ \mu\text{F}$ decoupling capacitor should be connected between V_{DD} and GND.
4. Measured with rail-to-rail input clock
5. Measured on rising edges at $V_{DD} \div 2$ between any two outputs with equal loading.

NB3L553

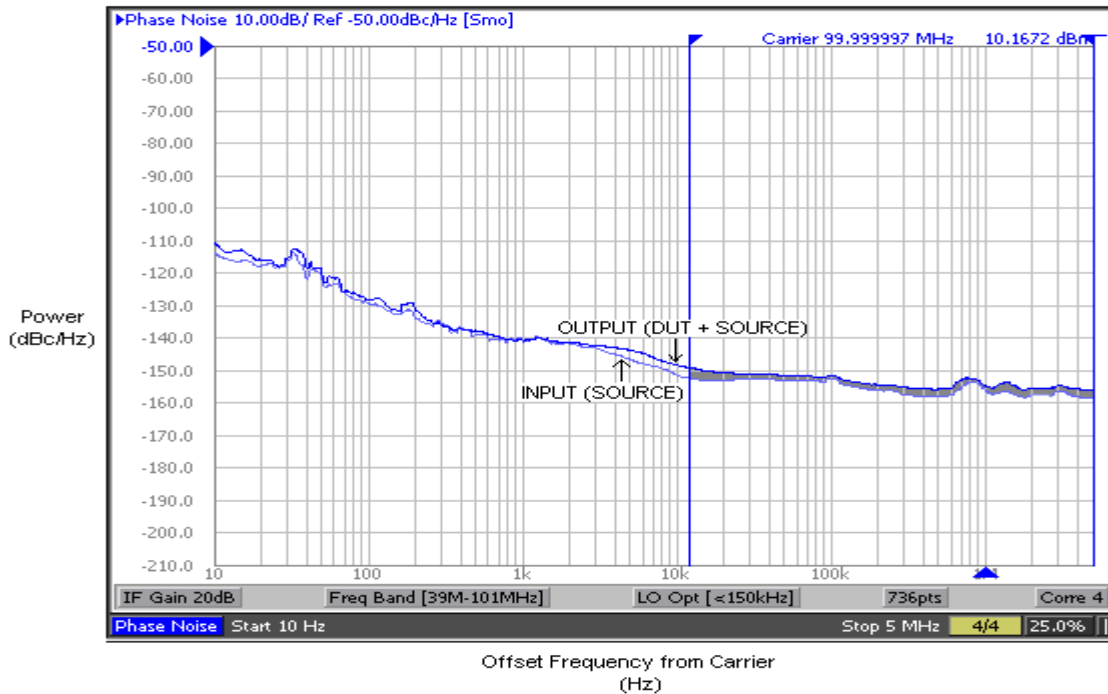


Figure 2. Phase Noise Plot at 100 MHz at an Operating Voltage of 3.3 V, Room Temperature

The above plot captured using Agilent E5052A shows Additive Phase Noise of the NB3L553 device measured with an input source generated by Agilent E8663B. The RMS phase jitter contributed by the device (integrated between 12 kHz to 20 MHz; as shown in the shaded area) is 18 fs (RMS Phase Jitter of the input source is 75.40 fs and Output (DUT+Source) is 93.16 fs).

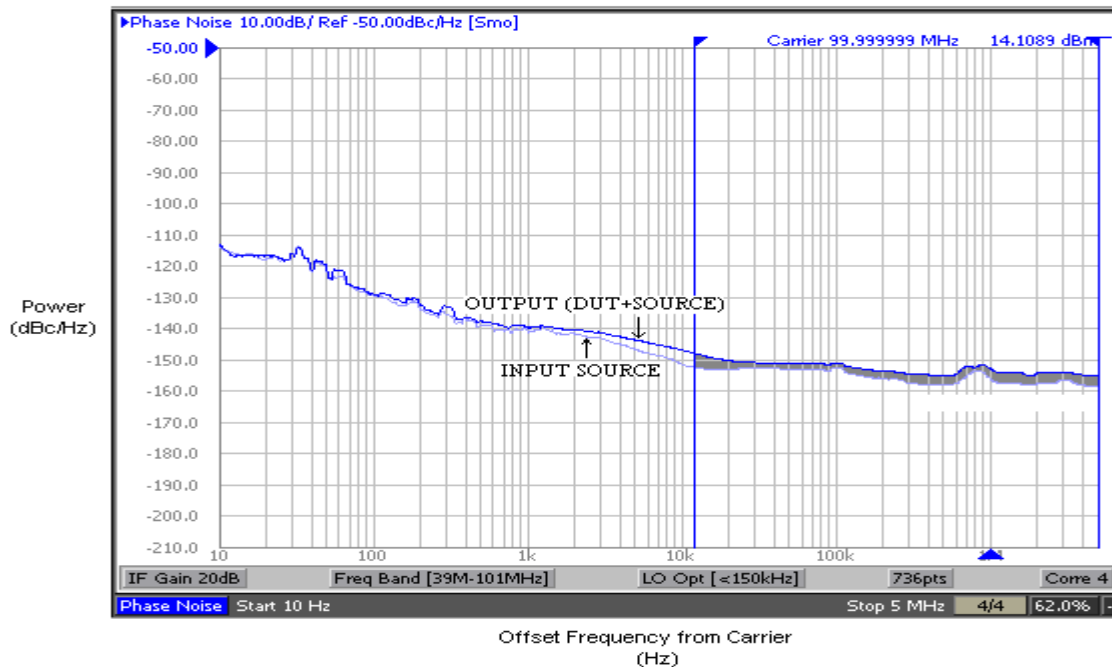


Figure 3. Phase Noise Plot at 100 MHz at an Operating Voltage of 5 V, Room Temperature

The above plot captured using Agilent E5052A shows Additive Phase Noise of the NB3L553 device measured with an input source generated by Agilent E8663B. The RMS phase jitter contributed by the device (integrated between 12 kHz to 20 MHz; as shown in the shaded area) is 29 fs (RMS Phase Jitter of the input source is 75.40 fs and Output (DUT+Source) is 103.85 fs).

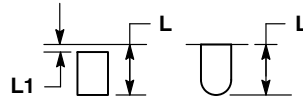
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016



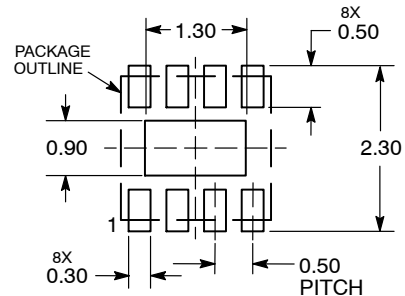
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.00 | BSC |
| D2 | 1.10 | 1.30 |
| E | 2.00 | BSC |
| E2 | 0.70 | 0.90 |
| e | 0.50 | BSC |
| K | 0.30 | REF |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |



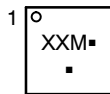
**RECOMMENDED
SOLDERING FOOTPRINT***



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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