

製品概要

NB6L11: Clock / Data Fanout Buffer / Translator, 2.5 V / 3.3 V Multilevel Input to 1:2 Differential LVPECL / LVNECL

技術情報は、データシートをご参照ください。

The NB6L11 is an enhanced differential 1:2 clock or data fan-out buffer/translator. The device has the same pin-out and is functionally equivalent to the LVEL11, EP11 and LVEP11 devices. Moreover, the device is optimized for the systems that require LOW skew, LOW jitter and LOW power consumtion. Differential input can be configured to accept single-ended signal by applying an external reference voltage to unused complementary input pin. Input accept LVNECL, LVPECL, LVTTL, LVCMOS, CML or LVDS. The outputs are 800mV ECL signals.

特長

- Input Clock Frequency 6 GHz
- · Input Data Rate 6 Gb/s
- · Low 14 mA Typical Power Supply Current
- 150 ps Typical Proagation Delay
- · 5 ps Typical Witin Device Skew
- 75 ps Typical Rise/Fall Times
- PECL Mode Operating Range: VCC = 2.375 V to 3.465 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -2.375 V to -3.465 V
- · Open Input Default State
- Q Outputs will default LOW with Inputs Open or at VEE For more features, see the data sheet

アプリケーション

- · Backplane Clock distribution
- Signal Translation Between LVDS, CML, LVTTL or LVCMOS to LVPECL

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