製品概要

NB7L86M: 2.5 V / 3.3 V, 12 Gb/s Differential Clock / Data Smart Gate with CML Output and Internal Termination

技術情報は、データシートをご参照ください。

The NB7L86M is a multi-function differential Logic Gate, whichcan be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1MUX. This device is part of the GigaComm family of highperformance Silicon Germanium products. The NB7L86M is anultra-low jitter multi-logic gate with a maximum data rate of 12 Gb/sand input clock frequency of 8 GHz suitable for Data CommunicationSystems, Telecom Systems, Fiber Channel, and GigE applications.The device is housed in a low profile 3x3 mm 16-pin QFN package.Differential inputs incorporate internal 50 Ω termination resistorsand accept LVNECL (Negative ECL), LVPECL (Positive ECL),LVCMOS, LVTTL, CML, or LVDS. The differential 16 mA CMLoutput provides matching internal 50 Ω termination, and 400 mVoutput swing when externally terminated 50 Ω to VCC.Application notes, models, and support documentation are availableon www.onsemi.com.

特長

- Maximum Input Clock Frequency up to 8 GHz
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 90 ps Typical Propagation Delay
- 2 ps Typical Within Device Skew
- CML Output with Operating Range: VCC = 2.375 V to 3.465 V with VEE = 0 V
- CML Output with Operating Range: VCC = 2.375 V to 3.465 V with VEE = 0 V
- CML Output Level (400 mV Peak-to-Peak Output) Differential Output
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP and SG Devices

  For more features, see the data sheet

アプリケーション

- Data routing in Data Communication Systems, Telecom Systems, Fiber Channel, and GigE applications.
- Clock multiplexing for redundancy

詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。

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