製品概要

MC100EPT21: Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

技術情報は、データシートをご参照ください。

The MC100EPT21 is a Differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL/LVDS/CML input levels and LVTTL/LVCMOS output levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal. The VBB output allows the EPT21 to be cap coupled in either single-ended or differential input mode. When single-ended cap coupled, VBB output tied to the D0 input for a non-inverting buffer or the D0 input for an inverting buffer. When cap coupled differentially, VBB output is connected through a resistor to each input pin. If used, the VBB pin should be bypassed to VCC via a 0.01 F capacitor. For additional information see AND8020. For a single-ended direct connection use an external voltage reference source such as a resistor divider. Do not use VBB for a single-ended direct connection.

特長

- 1.4ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- 24mA TTL outputs
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- The 100 Series Contains Temperature Compensation
- VBB Output
- New Differential Input Common Mode Range

アプリケーション

- Precision Clock Translation

電気的仕様

製品	Pricing ($/Unit)	Compliance	Status	Channels	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package Type
MC100EPT21DG		Pb-free Halide free	Active	1	LVDS ECL CML	TTL	3.3	350	1.4	900	SOIC-8
MC100EPT21DR2G		Pb-free Halide free	Active	1	ECL CML LVDS	TTL	3.3	350	1.4	900	SOIC-8
MC100EPT21DTG		Pb-free Halide free	Active	1	CML LVDS ECL	TTL	3.3	350	1.4	900	TSSOP-8
MC100EPT21DTR2G		Pb-free Halide free	Active	1	CML LVDS ECL	TTL	3.3	350	1.4	900	TSSOP-8
MC100EPT21MNR4G		Pb-free Halide free	Active	1	ECL CML LVDS	TTL	3.3	350	1.4	900	DFN-8

詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。

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